

## LS XGK Cnet

Supported Series: LS XGT series XGK CPU with communication module XGL-CH2A

Website: <http://www.lgjs.com/>

### HMI Setting:

Parameters	Recommended	Options	Notes
PLC type	LS XGK Cnet		
PLC I/F	RS232	RS232/RS485 4W	
Baud rate	115200	9600~115200	
Data bits	8	7, 8	
Parity	None	Even, Odd, None	
Stop bits	1	1	
PLC sta. no.	1	0 ~ 32	

Online simulator	YES	Pass-Through	YES
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### Device Address:

Bit/Word	Device type	Format	Range	Memo
B	PW_Bit	DDDDh	0 ~ 2047f	I/O device Bit
B	MW_Bit	DDDDh	0 ~ 2047f	Internal device Bit
B	LW_Bit	DDDDDh	0 ~ 11263f	Communication device Bit
B	KW_Bit	DDDDh	0 ~ 2559f	Preservation device Bit
B	FW_Bit	DDDDh	0 ~ 2047f	Special device Bit( write available from 1025)
B	DW_Bit	DDDDDh	0 ~ 32767f	Data register_Bit expression (D0000.0)
B	UW_Bit	DH.DDh	0 ~ 3f.31f	XGK-CPUE : hh(0~1f)
B	RW_Bit	DDDDDh	0 ~ 32767f	
B	ZRW_Bit	DDDDDh	0 ~ 32767f	
B	NW_Bit	DDDDDh	0 ~ 21503f	
B	ZW_Bit	DDh	0 ~ 127f	
B	SX	DDDDD	0 ~ 12799	Relay for step control Bit
B	TX	DDDD	0 ~ 2047	Timer device Bit
B	CX	DDDD	0 ~ 2047	Counter device Bit
W	PW	DDDD	0 ~ 2047	I/O device
W	MW	DDDD	0 ~ 2047	Internal device

Bit/Word	Device type	Format	Range	Memo
W	LW	DDDDD	0 ~ 11263	Communication device
W	KW	DDDD	0 ~ 2559	Preservation device
W	FW	DDDD	0 ~ 2047	Special device( write available from 1025)
W	DW	DDDDD	0 ~ 32767	Data register
W	UW	DH.DD	0.00 ~ 3f.31	Analog data register XGK-CPUE : hh(0~1f)
W	RW	DDDDD	0 ~ 32767	
W	ZRW	DDDDD	0 ~ 32767	
W	NW	DDDDD	0 ~ 21503	Communication data register
W	ZW	DDD	0 ~ 127	Index register_128 words
W	SW	DDDDD	0 ~ 127	Relay for step control
W	TW	DDDD	0 ~ 2047	Timer current value register
W	CW	DDDD	0 ~ 2047	Counter current value register

## Wiring Diagram:

XGL-CH2A CH1 RS232 9P D-Sub Male (Diagram 1~Diagram 3)

### Diagram 1

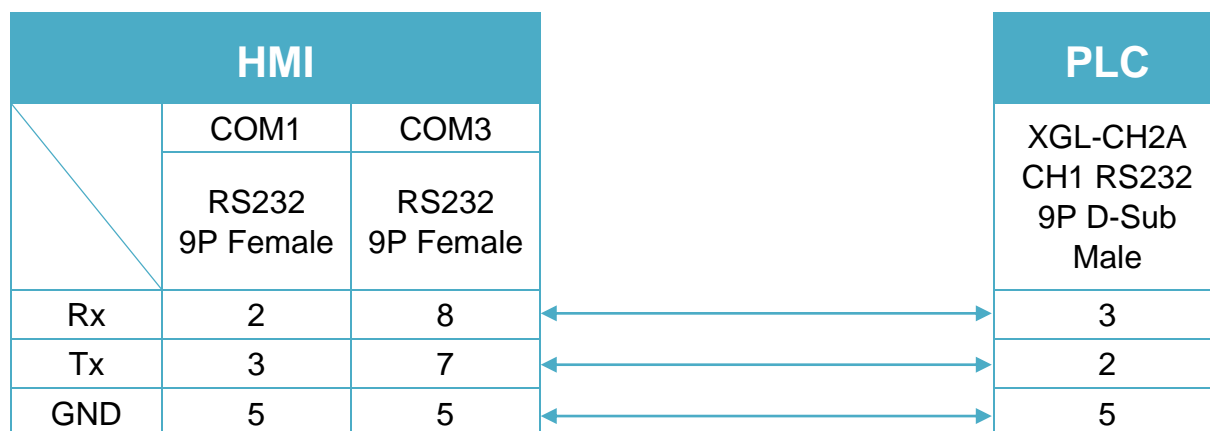
**cMT Series**                      *cMT3071 / cMT3072 / cMT3090 / cMT3103 / cMT3151*

**eMT Series**                      *eMT3070 / eMT3105 / eMT3120 / eMT3150*

**MT-iE**                              *MT8073iE / MT8102iE*

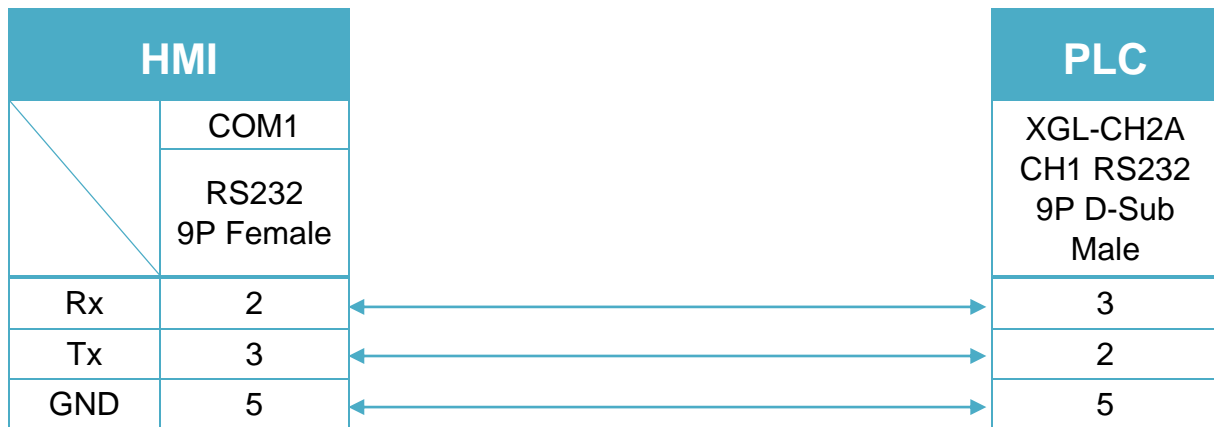
**MT-XE**                              *MT8092XE*

**MT-iP**                              *MT6103iP / MT8102iP*



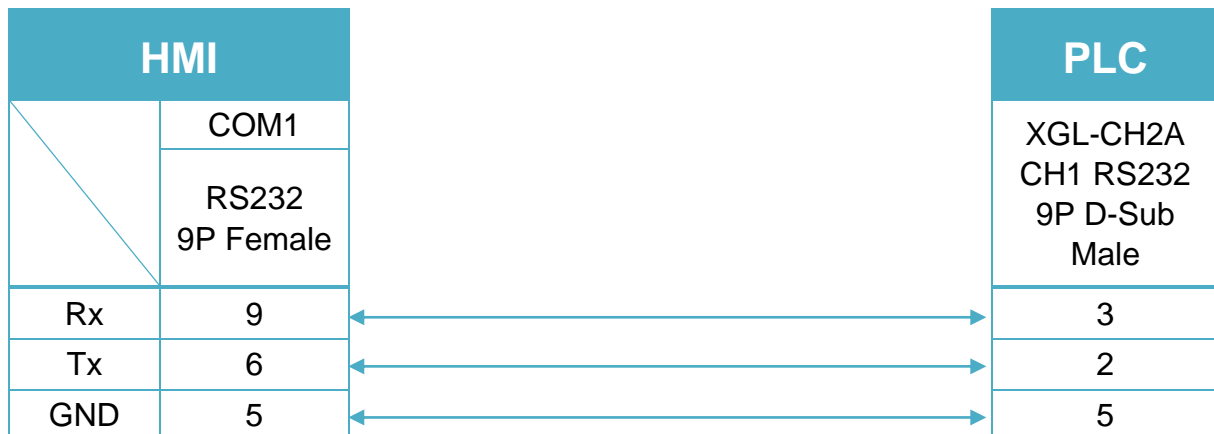
## Diagram 2

<b>cMT Series</b>	<b><i>cMT-SVR / cMT-G01 / cMT-G02 / cMT-HDM / cMT-FHD</i></b>
<b>mTV</b>	<b><i>mTV</i></b>
<b>MT-iE</b>	<b><i>MT8070iE / MT6070iE / MT8100iE / MT8121iE / MT8150iE / MT8071iE / MT6071iE / MT8072iE / MT6072iE / MT8073iE / MT8101iE / MT8102iE / MT8103iE</i></b>
<b>MT-XE</b>	<b><i>MT8121XE / MT8150XE / MT8090XE</i></b>



## Diagram 3

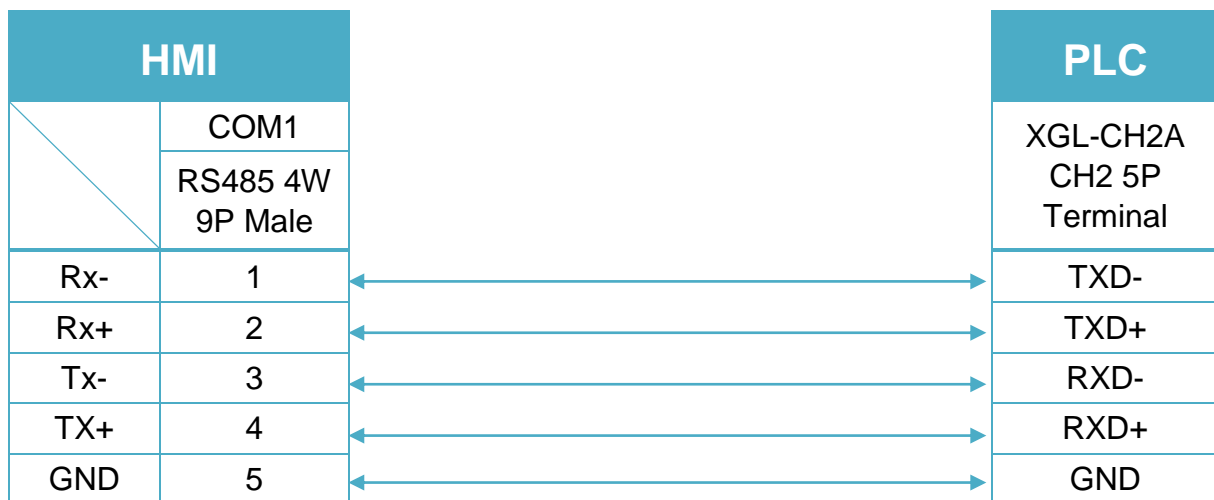
<b>MT-iE</b>	<b><i>MT8050iE / MT8053iE</i></b>
<b>MT-iP</b>	<b><i>MT6051iP / MT8051iP / MT6071iP / MT8071iP</i></b>



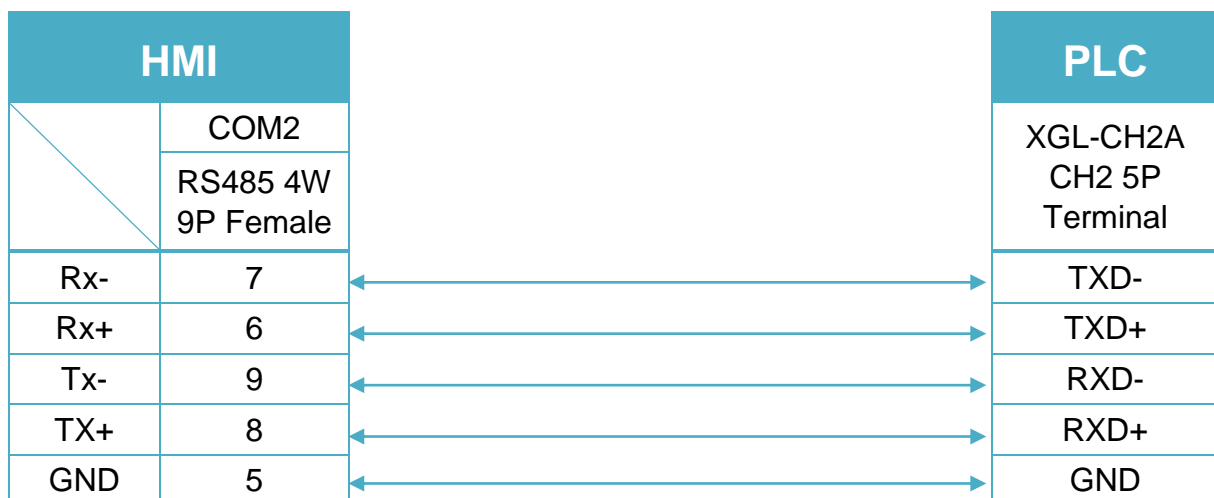
## XGL-CH2A CH2 5P Terminal (Diagram 4 ~ Diagram 7)

**Diagram 4**

<b>cMT Series</b>	<b><i>cMT3151</i></b>
<b>eMT Series</b>	<b><i>eMT3070 / eMT3105 / eMT3120 / eMT3150</i></b>
<b>MT-iE</b>	<b><i>MT8070iE / MT6070iE / MT8100iE / MT8121iE / MT8150iE</i></b>
<b>MT-XE</b>	<b><i>MT8121XE / MT8150XE</i></b>

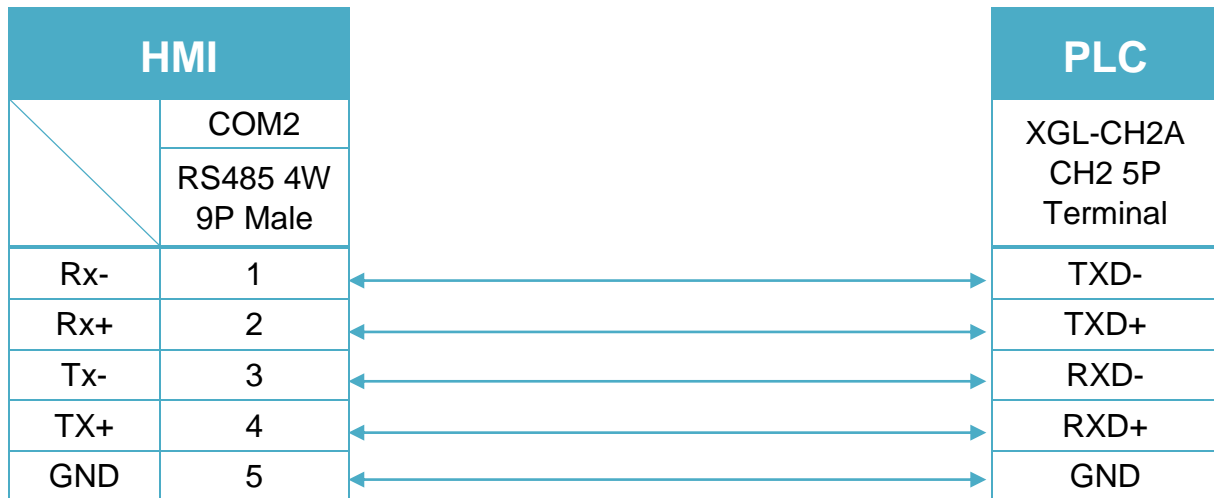

**Diagram 5**

<b>cMT Series</b>	<b><i>cMT-SVR / cMT-G01 / cMT-G02 / cMT-HDM / cMT-FHD</i></b>
<b>mTV</b>	<b><i>mTV</i></b>



## Diagram 6

<b>cMT Series</b>	<b><i>cMT3071 / cMT3072 / cMT3090 / cMT3103</i></b>
<b>MT-iE</b>	<b><i>MT8071iE / MT6071iE / MT8072iE / MT6072iE / MT8073iE / MT8101iE / MT8102iE / MT8103iE</i></b>
<b>MT-XE</b>	<b><i>MT8090XE / MT8092XE</i></b>
<b>MT-iP</b>	<b><i>MT6071iP / MT8071iP / MT6103iP / MT8102iP</i></b>



## Diagram 7

<b>MT-iE</b>	<b><i>MT8050iE / MT8053iE</i></b>
<b>MT-iP</b>	<b><i>MT6051iP / MT8051iP</i></b>

