LS XGK FEnet (Ethernet)

Supported Series: LS XGT series XGK CPU with XGL-EFMT Ethernet module.
Website: http://www.lgis.com/

HMI Setting:

Parameters	Recommended	Options	Notes
PLC type	LS XGK FEnet (Ethernet)		
PLC I/F	Ethernet		
Port no.	2004		

Device Address:

Bit/Word	Device type	Format	Range	Memo
B	PW_Bit	DDDDh	0 ~ 2047f	I/O device Bit
B	MW_Bit	DDDDh	0 ~ 2047f	Internal device Bit
B	LW_Bit	DDDDDh	0 ~ 11263f	Communication device Bit
B	KW_Bit	DDDDh	0 ~ 2559f	Preservation device Bit
B	FW_Bit	DDDDh	0 ~ 2047f	Special device Bit(write available from 1025)
B	SW_Bit	DDDDDh	0 ~ 12799	Relay for step control Bit
B	DW_Bit	DDDDDh	0 ~ 32767f	Data register_Bit expression (D0000.0)
B	UW_Bit	DH.DDh	0 ~ 3f.31f	XGK-CPUE : hh(0~1f)
B	RW_Bit	DDDDDh	0 ~ 32767f	
B	ZRW_Bit	DDDDDh	0 ~ 32767f	
B	NW_Bit	DDDDDh	0 ~ 21053f	
B	ZW_Bit	DDDh	0 ~ 127f	
B	TX	DDDD	0 ~ 2047	Timer device Bit
B	CX	DDDD	0 ~ 2047	Counter device Bit
W	PW	DDDD	0 ~ 2047	I/O device
W	MW	DDDD	0 ~ 2047	Internal device
W	LW	DDDDD	0 ~ 11263	Communication device
W	KW	DDDD	0 ~ 2559	Preservation device
W	FW	DDDD	0 ~ 2047	Special device(write available from 1025)
W	SW	DDDDD	0 ~ 127	Relay for step control
W	DW	DDDDD	0 ~ 32767	Data register
W	UW	DH.DD	0.00 ~ 3f.31	Analog data register XGK-CPUE : hh(0~1f)

Bit/Word	Device type	Format	Range	Memo
W	NW	DDDDD	0 ~ 21503	Communication data register
W	ZW	DDD	0 ~ 127	Index register_128 words
W	TW	DDDD	0 ~ 2047	Timer current value register
W	CW	DDDD	0 ~ 2047	Counter current value register
W	RW	DDDDD	0 ~ 32767	
W	ZRW	DDDDD	0 ~ 32767	

Wiring Diagram:

Ethernet cable: